Node Based Clock Gating: Reducing NoC Power

Kyurae Lee, Wooil Kim

System LSI Business, Samsung Electronics Co., Ltd

Motivation

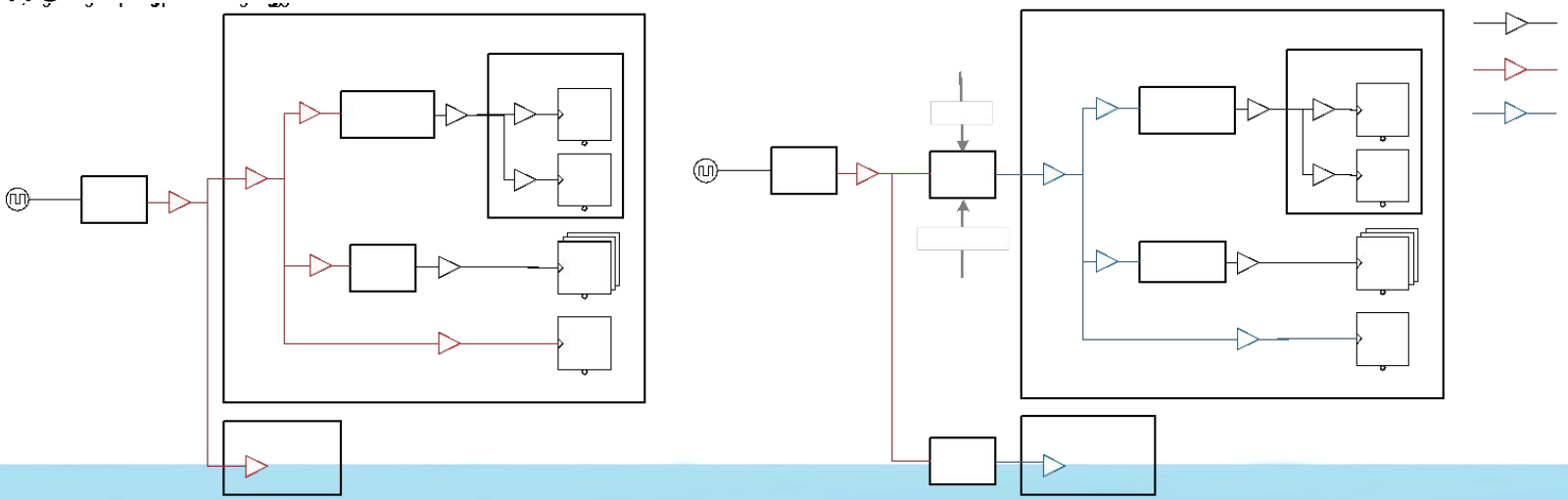
- Need power reduction for light access patterns
  - Mobile System on Chips (SoCs) have various usage patterns, with one being the 'Day-of-Use' pattern, which consists of
    - A few intensive access patterns
      - Video recording
      - NPU processing
    - Mostly light access patterns
      - Web browsing
      - Using SNS
      - Video streaming
  - Many proposals for clock gating schemes were introduced, but they were still not effective for ‘mostly light access patterns’

Motivation

- Limitation of Previous Proposals
  - Automated hardware-driven Clock Gating (ACG)
    - A technique that gates the clock source when a NODE is in an IDLE state, making it highly power effective. However, it may not be suitable for low-bandwidth scenarios because it cannot gate the clock when less traffic is periodically transferred through the NODEs
  - Instantiated/inferred clock gating
    - Provides designer-intentioned clock gating, which results in efficient clock gating. However, clock gating granularity is small because clock gating enable conditions should be suitable for efficient clock enable
  - Effective clock gating for a low bandwidth scenario cannot fully be achieved because of these limitations

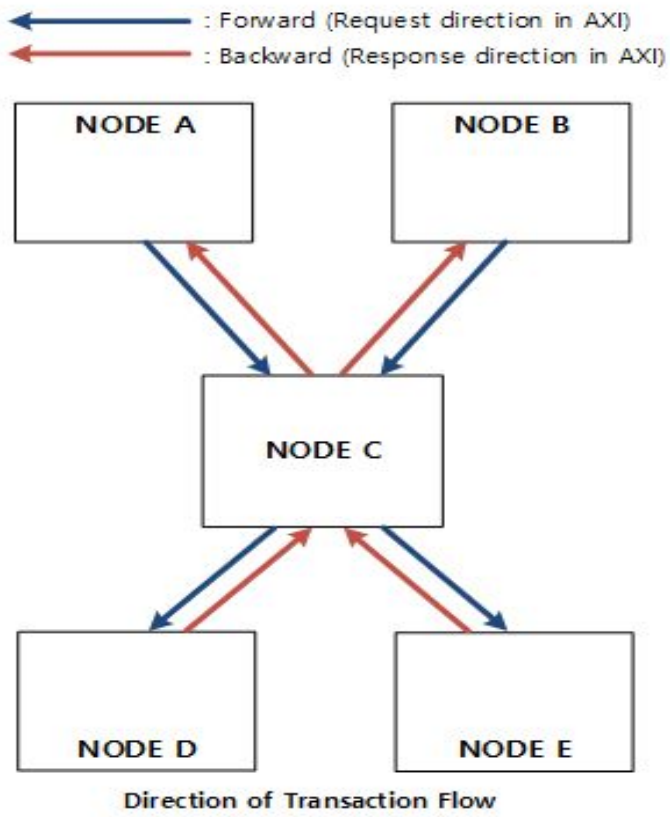
Main Idea: *Node Based Clock Gating*

- Insert Node Based Clock Gating (NBCG) logic between ACG and Instantiated or inferred clock gating logics
  - The following figure describes clock gating coverage before and after inserting NBCG logic into a dedicated NODE
    - Blue highlight clock trees have chances to be clock gated even though there is some traffic



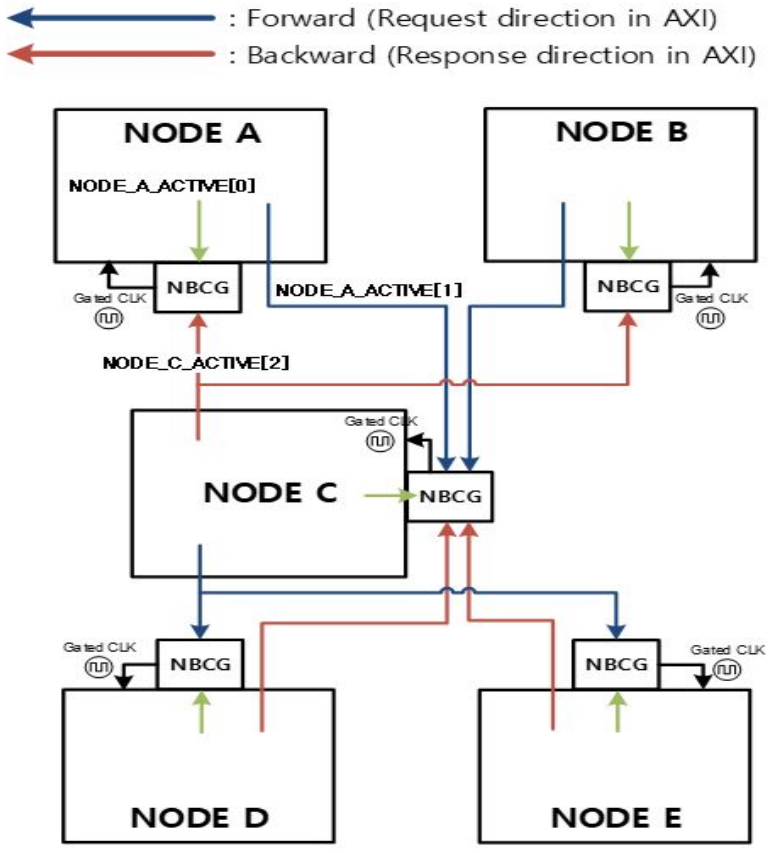
Main Idea: *Node Based Clock Gating*

- Condition
  - The NoC (Network-on-Chip) consists of multiple function modules, which we propose to call 'NODEs'
  - NoC with deterministic routing
  - AXI protocol has separate request and response channels
    - The blue line indicates the forward (Request in AXI) direction
    - The red line indicates a backward (Response in AXI) direction



Main Idea: *Node Based Clock Gating*

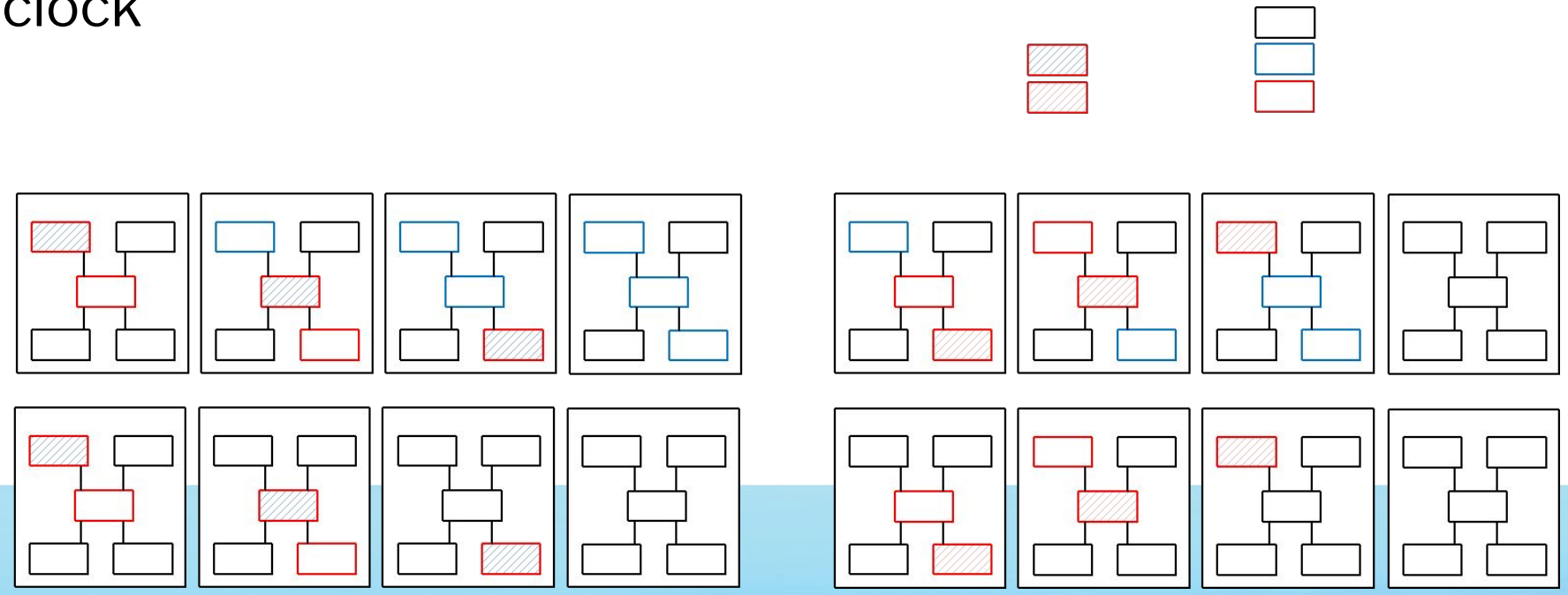
- Implementation
  - The activation signals for each NODE consist of 3-bit signals, named as 'NODE_ACTIVE[2:0]
    - NODE_ACTIVE[0] enables the clock of the NODE itself only. (Green line)
    - NODE_ACTIVE[1] enables NBCG components to enable the clock of both the 1) NODE itself and 2) adjacent NODE in the forward direction. (Blue line)
    - NODE_ACTIVE[2] enables the NBCG components to enable the clock of both the 1) NODE itself and 2) adjacent NODE in a backward direction. (Red line)
  - Using separate activation signals allows for appropriate and effective clock gating of each NBCG component



NBCG with Activate Signals and Gated Clock

Main Idea: *Node Based Clock Gating*

- Comparison against existing clock gating schemes
  - NoC with deterministic routing
  - AXI protocol
  - Blue highlight NODEs are clock enabled even though they actually do not require clock



Main Idea: *Node Based Clock Gating*

- NBCG provides and resolves
  - In the conventional AXI protocol with deterministic routing, it is hard to gate the clock for NODEs when there are outstanding requests
    -> Resolves this restriction by adopting active signals from the NODE itself and adjacent NODEs
  - No need to send or manage additional signals or transactions to notify early wake-up between NODEs (like FLITPEND in the CHI protocol)
    -> NBCG is automatically hardware-driven
  - NBCG receives not only active information from its own NODE but also information from adjacent NODEs
    -> Enabling the clock earlier without any additional latency

Evaluation

Power Evaluation Environment

- NoC structure: 46-input/4-output (46x4) multi-layered switch, 32-byte data width
- Memory subsystem: Four-channel interleaved memory
- Operating frequency: 936MHz
- Clock gating scheme: ACG, instantiated CG, inferred CG, and proposed NBCG
- Requesters: Camera, NPU, Display, and Modem
- Used bandwidth (Ideal BW = 240GB/s)
  Scenario 1) 13.68GB/s (Utilization = 5.71%)
  Scenario 2) 23.36GB/s (Utilization = 9.75%)
  Scenario 3) 35.40GB/s (Utilization = 14.77%)
- Power evaluation tool: PowerArtist with RTL simulation result

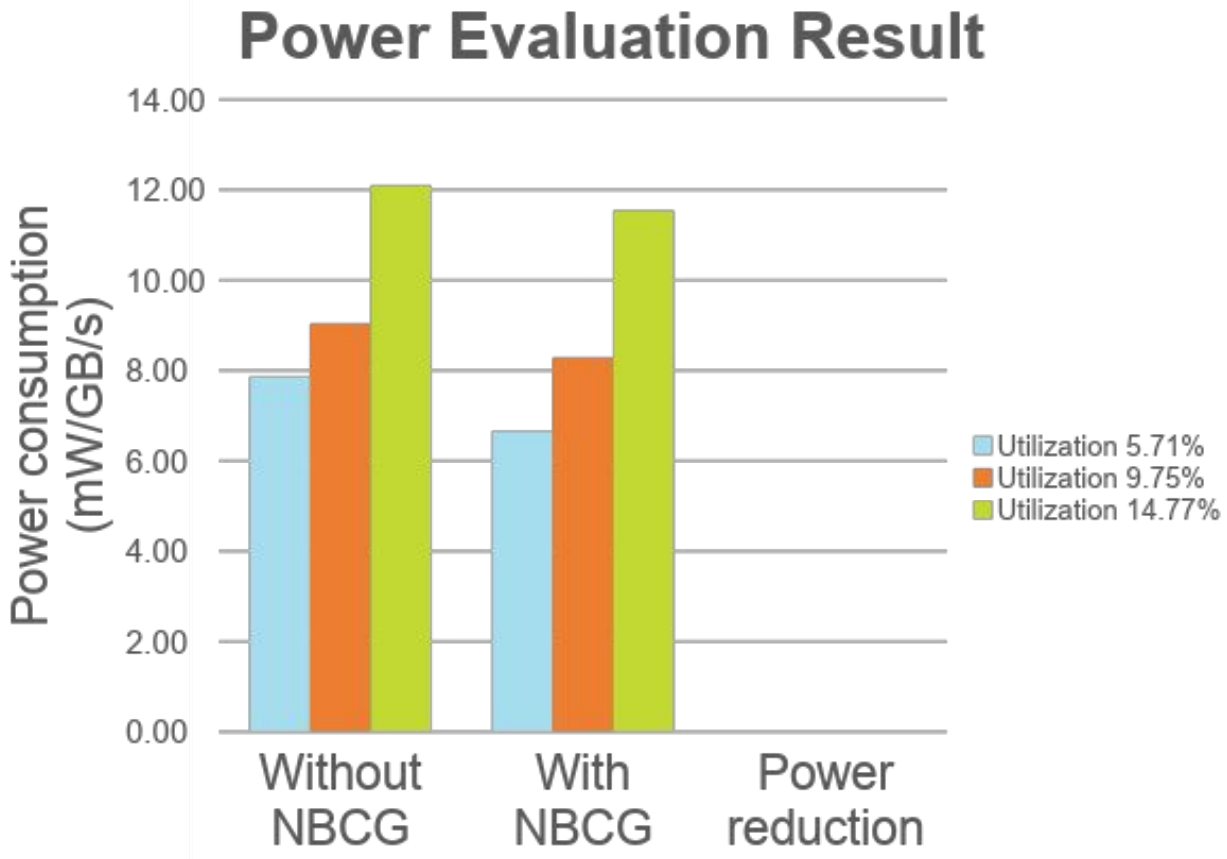
Synthesis Environment for Area

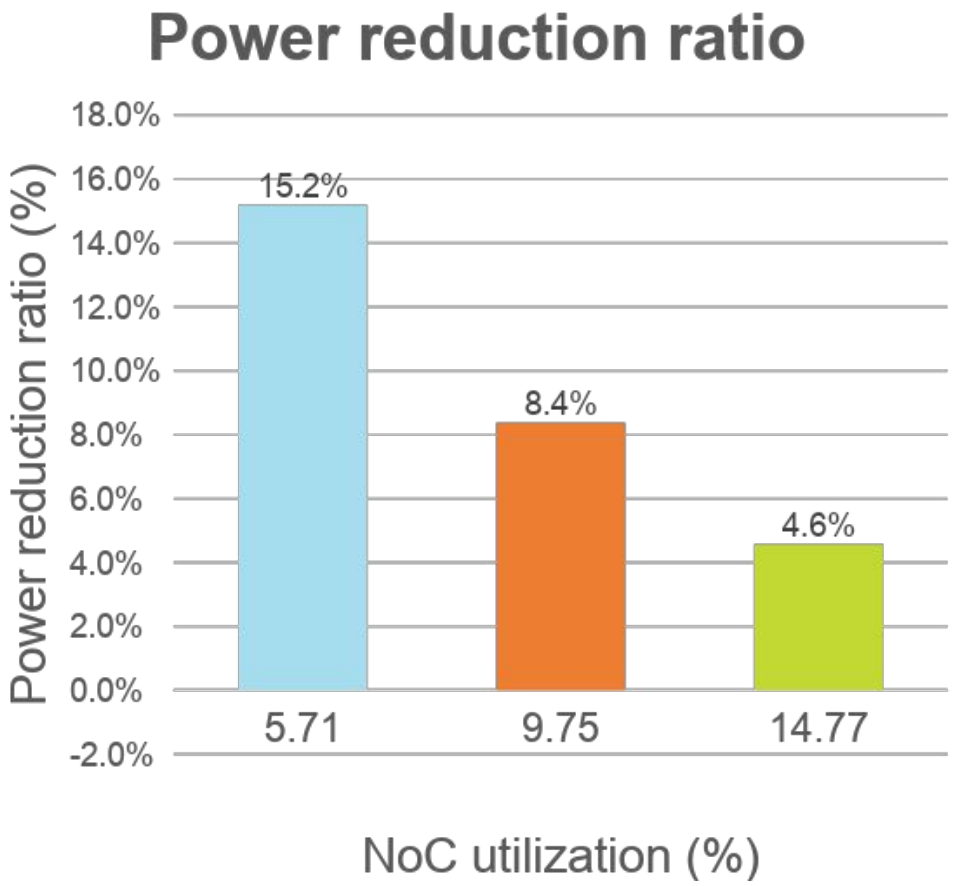
- Technology: Samsung 4LPE
- Target Frequency: 1GHz

Synthesis Result

NBCG	Area Ratio
Not applied	100%
Applied	100%

Evaluation


Power Evaluation Result
Power consumption (mW/GB/s)
14.00
12.00
10.00
8.00
6.00
4.00
2.00
0.00
Without NBCG
With NBCG
Power reduction
Utilization 5.71%
Utilization 9.75%
Utilization 14.77%


Power reduction ratio
Power reduction ratio (%)
18.0%
16.0%
14.0%
12.0%
10.0%
8.0%
6.0%
4.0%
2.0%
0.0%
-2.0%
15.2%
8.4%
4.6%
5.71
9.75
14.77
NoC utilization (%)

Summary

Motivation

- Modern mobile SoCs require low-power features to improve battery life. The Day-of-Use pattern includes a few intensive access patterns and mostly light access patterns.
- The effective clock gating of the NoC for low-bandwidth scenarios cannot be fully achieved due to the limitations of existing clock gating proposals.

Challenges

- The previously proposed clock gating methodologies cannot effectively cover clock gating in low-bandwidth scenarios.
- Less additional latency is required for implementing additional clock gating.
- Our clock gating approach is area-efficient, requiring less area overhead.

Solution

- We propose Node Based Clock Gating (NBCG) to reduce NoC power consumption during low-bandwidth scenarios with no area or latency overhead.
- Our evaluation shows that NBCG improves NoC power consumption by 15.1% in low-bandwidth scenarios with no timing or latency overhead.
- The proposed NBCG approach can be adopted not only for NoC but also for other components of mobile SoCs.